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A Completely Integrated 1.9-GHz Receiver Front-End With Monolithic Image-Reject Filter and VCO

John W. M. Rogers, José A. Macedo, and Calvin Plett

***Abstract*—A 1.9-GHz monolithic superheterodyne receiver front-end with 300-MHz IF on-chip tunable image-reject filter and voltage-controlled oscillator (VCO) is presented. Two versions of the receiver were fabricated on a 0.5-μm bipolar process and compared to a previously fabricated version with an off-chip VCO. The two versions are identical, except for the fact that the 2.2-GHz VCO was realized with and without ground-shielded inductors. The receiver that used ground-shielded inductors had a conversion gain of 25.6 dB, a noise figure of 4.5 dB, a third-order input intercept point (IIP3) of −19 dBm, an image rejection of 65 dB, and a phase noise of −103 dBc/Hz at 100-kHz offset. The receiver drew 32.5 mA from a 3-V supply and had a die area of 2.1 mm $\times$ 1.7 mm. The local-oscillator–IF isolation improved compared to the previously fabricated front-end with an off-chip VCO.**

***Index Terms*—Inductors, integrated circuit design, MMIC receivers, notch filters, voltage-controlled oscillator.**

I. Introduction

Superheterodyne receivers are state-of-the-art in mobile communications [1]. A superheterodyne receiver front-end consists of a low-noise amplifier (LNA), an image filter, a mixer, and a voltage-controlled oscillator (VCO), as shown in Fig. 1. An LNA with a very low noise figure (NF) is typically required to enable the receiver to detect very weak signals. Additionally, the LNA must provide sufficient gain to suppress the noise generated by the following stages (image filter and mixer). The image filter is required to suppress the unwanted image frequency, which is located two IFs away from the desired RF [2]. The mixer translates the desired signal from the RF to an IF, usually a lower frequency, for further processing by the receiver back-end. Finally, the VCO allows channel selection of signals in the receive band.

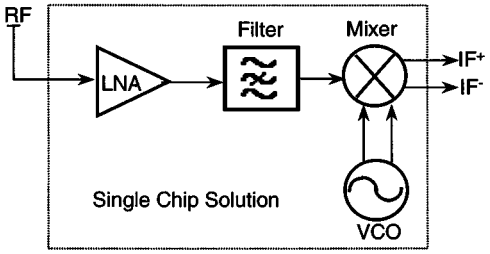

Fig. 1. Block level diagram of a superheterodyne receiver front-end.

Currently, off-chip passive filters, such as surface acoustic-wave (SAW) filters or ceramic filters, are used for image rejection. Recent work has shown, however, that it is possible to integrate the image filter on-chip using either an image-reject mixer [3], [4] or with the use of an image-reject notch filter [5]–[7] It is also typical to use off-chip VCOs or VCOs with off-chip resonators due to the low-Q of on-chip inductors. These filters and VCOs represent the major impediment to raising the level of integration of wireless radios since they cannot be easily implemented monolithically. They also represent a significant fraction of the overall cost of the receiver front-end.

To avoid the cost and complexity of going off-chip between individually packaged components, it is desirable to integrate as many components as possible. Previously it has been shown that it is possible to integrate the image filter on-chip. In this paper, the receiver previously presented in [5] is expanded to include a VCO. This work demonstrates that it is possible to integrate a superheterodyne receiver front-end (LNA, on-chip image filter, and mixer) with a VCO without impacting its performance. Further, the VCO's performance is shown to be improved by the use of inductors with a slotted ground shield that improve their Q. The result of this study is an RF front-end with no off-chip components, except for the input matching elements (only one series inductor).

II. Circuit Building Blocks

An integrated superheterodyne receiver front-end containing an LNA, an image-reject filter, and a mixer was previously developed [5]. This receiver front-end was tested with an off-chip local oscillator (LO) (implemented with an RF signal generator).

The purpose of this paper is to further the integration level of the described superheterodyne receiver by integrating the VCO on-chip. This then ensures the minimum number of RF pins, only one RF input and two IF outputs (differential).

The complete schematic of the integrated receiver consisting of an LNA, a tunable image filter, a mixer, and a VCO is shown in Fig. 2. The buffers (emitter followers) at the IF outputs and the dc bias of Q_1 and Q_2 have been omitted and I_3, I_6, I_{15}, I_{16}, I_{17}, and I_{18} are shown as ideal sources for simplicity.

The receiver front-end is designed for a 1.9-GHz RF input and a 300-MHz IF. A high-sided LO of 2.2 GHz is selected and the image, therefore, lies at 2.5 GHz, which is rejected by the image filter.

Manuscript received December 10, 2000; revised February 16, 2001. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada and by MICRONET.

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Publisher Item Identifier S 0018-9480(02)00734-2.

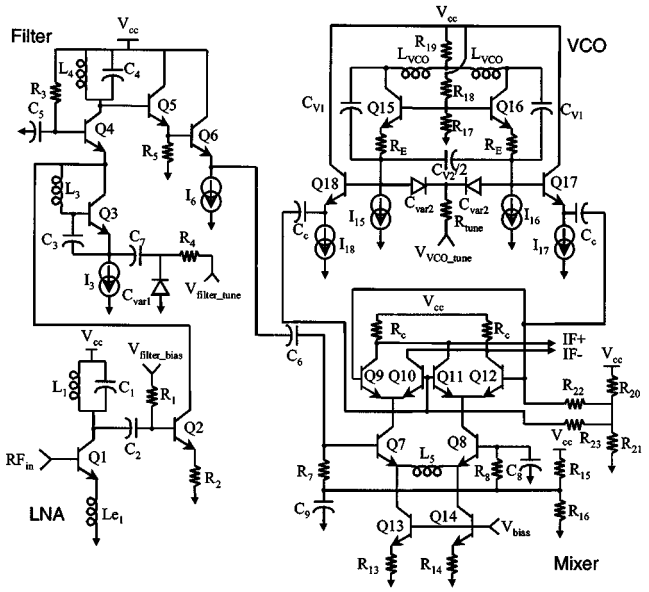

Fig. 2. Complete schematic of the receiver front-end.

A. Design of the LNA and Down-Conversion Mixer

A common-emitter topology was selected for the LNA in order to minimize the NF while obtaining good gain [8]. The LNA consists of transistor Q_1 with an *LC* resonant tank at the collector (L_1 and C_1) and emitter degeneration provided by inductor L_{e1}. Components L_1 and C_1 were selected to resonate at 1.9 GHz to provide the desired passband response. In order to minimize base resistance, a large ($80\ \mu\text{m} \times 0.5\ \mu\text{m}$) emitter transistor was selected for the LNA and was biased at 3 mA.

The double-balanced mixer consists of the input differential pair Q_7, Q_8 with inductive degeneration (L_5) for reduced noise and the quad Q_9, Q_{10}, Q_{11}, and Q_{12}. The RF signal available at the filter output (emitter of Q_6) is ac coupled to the base of Q_7 by means of capacitor C_6. This single-ended RF signal is then converted into in-phase and antiphase currents by the differential transistor pair Q_7, Q_8 and fed to the upper four switching transistors Q_9, Q_{10}, Q_{11}, and Q_{12}. The switching quad is driven by the 2.2-GHz differential LO signal, which is generated by the on-chip VCO. Observe that the VCO signal is ac coupled to the bases of the switching transistors by means of capacitors (C_c).

The emitter degeneration inductor L_5 achieves a substantial reduction in noise while providing improved linearity. To ensure symmetry, L_5 was made out of two identical inductors to realize a total inductance of 14 nH. The mixer input transistors Q_7 and Q_8 were selected as large size devices (a 80 μm $\times$ 0.5 μm emitter) for reduced noise. They are biased at 1.25 mA each by means of current sources (Q_{13} and Q_{14}) whose current is adjusted by means of V_{bias}. The switching quad transistors were made one-half the size of the input pair transistors to ensure fast switching while still maintaining low noise. Collector load resistors (R_c) were selected to ensure sufficient conversion gain. The IF outputs (IF+ and IF−) are fed into two emitter follower buffers (which, for simplicity, are not shown in the schematic of Fig. 2), which can drive 50-Ω loads for testing purposes.

B. Design of the Image-Reject Filter

The image-reject filter consists of transistors Q_2, Q_3, and Q_4. Transistor Q_2 is biased at 2.5 mA. The series (notching) resonator consists of L_3, Q_3, C_3, C_7, and C_{var1}, which is used to tune the notch to 2.5 GHz. An *LC* tank (L_4, C_4) has been added to the collector of Q_4 to tune the passband for 1.9-GHz operation. Thus, the frequency response from the base of Q_2 to the collector of Q_4 will exhibit a passband response at 1.9 GHz and a notch at 2.5 GHz. The passband adds gain to the desired RF signal while the notch suppresses the undesired image. The cascoded amplifier output is buffered with a pair of emitter followers (Q_5, Q_6) to isolate it from the mixer stage that follows so that the mixer load does not detune or reduce the gain of the filter response.

The filter has a pair of complex zeros providing a notch in the transfer function with resonant frequency ω_z given by

$$\omega_z = \frac{1}{\sqrt{L_3 \cdot \left[\dfrac{(C_{\pi 3} + C_3)C_v}{(C_{\pi 3} + C_3) + C_v}\right]}} \tag{1}$$

where C_v represents the total capacitive load at the emitter of transistor Q_3.

Thus, based on (1), the designer can first select the value for L_3 (in this application, 3.5 nH) and then adjust the values of C_{var1} and C_3 to obtain the desired resonance (in this design, C_3 was 2.5 pF), C_7 serves mainly as a coupling capacitor and can be made relatively large (in this design, 4 pF). In practice, this frequency centering is done with the help of an RF simulator using accurate models for the devices involved, as well as including the parasitic capacitances due to the layout. In the present receiver, ω_z is designed to be centered at 2.5 GHz, which is the frequency of the undesired image.

The depth of the notch is controlled by adjusting g_{m3} by means of current I_3. The value of I_3, which complies with the above equation, is referred to as $I_{3\text{normal}}$ and ensures the deepest notch. If the current I_3 is increased significantly beyond the normal operation value ($I_{3\text{normal}}$), the circuit can be made to oscillate. It can be shown that the limit is approximately given by

$$I_{3\text{oscill}} = I_{3\text{normal}} \left(\frac{R + r_{e4}}{R}\right) \tag{2}$$

where R represents the total series losses of the on-chip inductor L_3 and the base resistance of transistor Q_3. This ensures robustness against undesired oscillation due to variations in the tuning current I_3. For example, for the design implemented here, r_{e4} is approximately 8.6 Ω (3 mA through cascode Q_4), while R is in the order of 10 Ω (mainly due to the series resistance of the 3.5-nH monolithic inductor with a Q of approximately 5). Thus, the current I_3 would need to be increased beyond 1.86 times the current under normal operation to start oscillation. This has been experimentally verified.

C. Design of the VCO

The VCO is a differential implementation of a Colpitts common-base topology [9]. It uses capacitors C_{V1} and C_{V2} in parallel with the varactors to form a negative resistance feedback loop to cause oscillation. Output buffers have been added to the circuit to lower the loading on the VCO by the mixer. The VCO is tuned by means of the $V_{\text{vco\_tune}}$ control voltage.

The basic operation of the core of the oscillator can be described as follows. First of all, to ensure that oscillations begins, the following condition must be satisfied:

$$r_s < \frac{g_m}{\omega_{\text{osc}}^2 C_{V1}(C_{\text{var2}} + C_{V2})} \tag{3}$$

where r_s is the equivalent series resistance of the resonator. This equation sets a lower limit for g_m and, hence, the current to start oscillations.

The frequency of oscillation can be set by choosing the inductor and tank capacitance to resonate at the desired frequency. The frequency of oscillation is given by

$$\omega_{\rm osc} \approx \frac{1}{\sqrt{L_{\rm VCO}\left(\dfrac{C_{V1}(C_{V2}+C_{\rm var2})+C_{V1}C_{\pi}}{C_{V1}+C_{V2}+C_{\rm var2}+C_{\pi}}+C_{\mu}\right)}}. \quad (4)$$

Having described the basic operation of the oscillator, this circuit must be carefully optimized if it is to have a high-Q tank and, therefore, low phase noise. The two major limiting factors that determine the equivalent parallel resistance of the tank are the dynamic emitter resistance (r_e) of the transistors Q_{15} and Q_{16} and the equivalent parallel resistance of the on-chip inductors. The addition of emitter degeneration (R_E) is used in an attempt to reduce the effect of the first loss, and ground-shielded inductors [10] are used in an attempt to increase the Q of the monolithic inductors. The equivalent parallel resistance of the tank can be approximated as

$$\frac{1}{R_{\rm Tank}} = \frac{1}{Q_{\rm ind}\omega_{\rm osc}L_{\rm VCO}} + \frac{1}{\left((r_e+R_E)\left(1+\dfrac{C_{V2}+C_{\rm var2}}{C_{V1}}\right)^2\right)} \quad (5)$$

where $Q_{\rm ind}$ is the Q of the inductor, r_e is the dynamic emitter resistance, and $C_{\rm var2}$ is the capacitance of the varactor. Thus, from (5), it can be seen that making $C_{V2}+C_{\rm var2}$ large and C_{V1} small will lead to a higher $R_{\rm Tank}$ and, therefore, a higher Q of the VCO. However, pushing this ratio too far could reduce the feedback to the point where the oscillator does not have enough gain to start.

In addition, low-frequency noise present on the terminals of the varactor can also be a limiting factor on the performance of the oscillator [10]. Thus, if the designer is not careful, this source of noise can dominate over other sources of noise in the oscillator. Thus, care was taken to keep the low-frequency noise on these terminals to a minimum. The phase noise of the oscillator can be calculated using the following formula [9], [12]:

$$L(f_m) = 10\log\left(\left(\frac{f_o}{2Qf_m}\right)^2\left[\frac{FkT}{2P_s}\left(1+\frac{f_c}{f_m}\right)\right] + \frac{1}{2}\left(\frac{K_{\rm VCO}V_m}{2f_m}\right)^2\right) \quad (6)$$

where $L(f_m)$ is the phase noise in decibels with respect to the carrier in a 1-Hz bandwidth f_o is the frequency of oscillation in hertz, f_m is the frequency offset from the carrier in hertz, F is the NF of the transistor amplifier, k is Boltzmann's constant in joules/kelvin, T is the temperature in kelvin, P_s is the RF power produced by the oscillator in watts, and f_c is the flicker noise corner frequency in hertz, $K_{\rm VCO}$ is the gain of the VCO in hertz/volt, and V_m is the total amplitude of all low-frequency noise sources in volts/$\sqrt{\text{hertz}}$.

Since the VCO function in this application was to drive a mixer, it was required to produce sufficient output voltage to adequately drive the mixer. If the VCO were to produce poor output voltage swing, then the quad of the mixer would not be fully switched, and this can lead to a degradation in the receiver NF and conversion gain. From [13], it can be shown that the output voltage swing of this oscillator can be given by

$$V_{\rm out} \approx 2A_f\left(\frac{C_{V1}}{C_{V1}+C_{V2}+C_{\rm var2}}\right)I_{15} \times\left(1-\frac{C_{V1}}{C_{V1}+C_{V2}+C_{\rm var2}}\right)(R_{\rm Tank,L}\parallel R_{\rm load}) \quad (7)$$

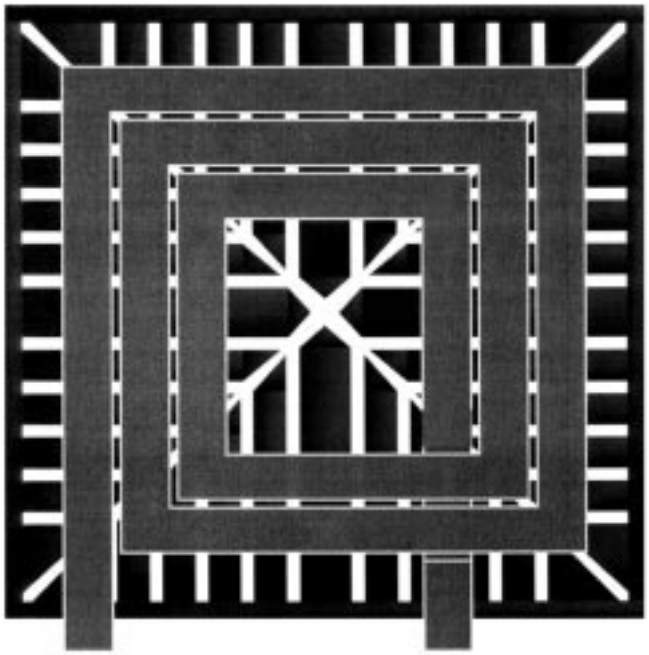

Fig. 3. Inductor with slotted ground shield used to reduce substrate losses.

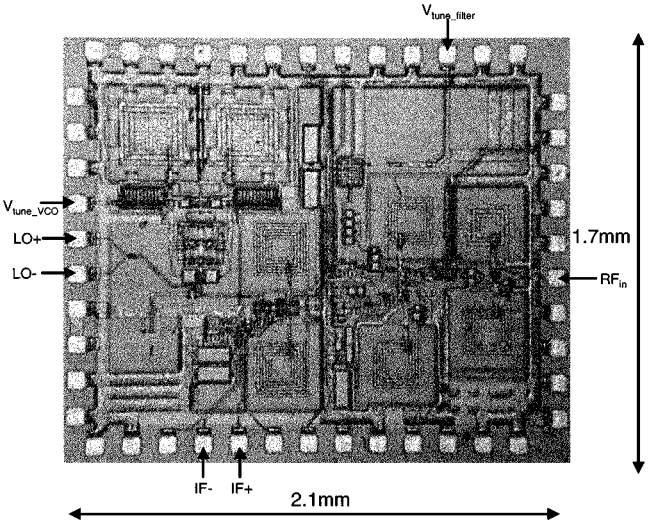

Fig. 4. Photomicrograph of the superheterodyne receiver front-end in a 0.5-mm silicon bipolar process.

where A_f is the loss due to the followers, $R_{\rm Tank,L}$ is the resistance in parallel with the tank due to the inductor, and $R_{\rm load}$ is the resistance presented to the tank by the load. This clearly shows the additional advantage of higher output voltage if the inductor losses are minimized.

III. Inductors

Unfortunately, on-chip inductors suffer from very limited Q's. This is due primarily to two factors. First, most bipolar technologies have high metal resistance even in their top level metal, and this limits the Q. At higher frequencies, the effective resistance of the inductor is further increased because of its proximity to a relatively lossy substrate. This is because the inductor capacitively couples signals into the substrate and stirs up eddy currents through magnetic coupling. Nothing can be done about the series resistance without altering the process [14]; however, the substrate loss can be reduced by placing a slotted ground-shield underneath the inductor, as shown in Fig. 3 [10]. This

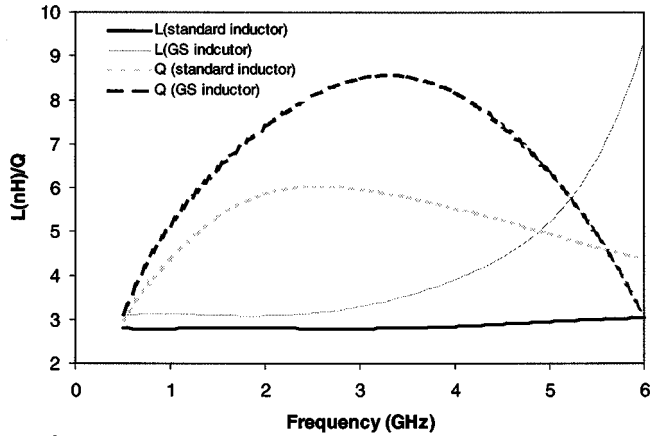

Fig. 5. Measurements of a standard and ground-shielded inductor.

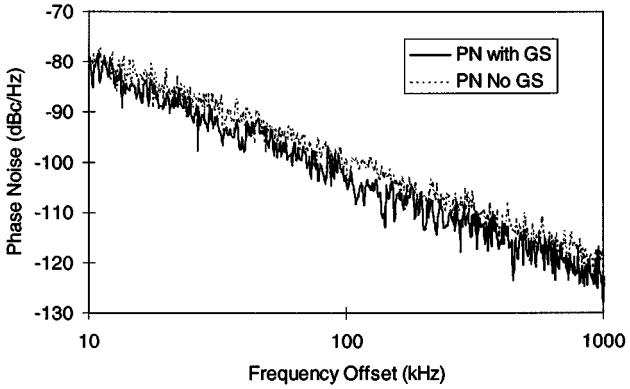

Fig. 6. Comparison of VCO phase noise (regular inductors versus ground-shielded inductors).

essentially replaces a lossy or low-Q capacitor with a much higher Q capacitor (although a larger one). The choice of layer used in the process to form the ground shield is also very important. In the technology used in this study, a layer of polycrystalline silicon that lies just below the silicon/silicon–dioxide interface was chosen because of its relatively low resistivity and vertical distance from the top level metal that forms the inductor.

In order to get the best performance from the inductor, it must be properly optimized using a simulation tool like ASITIC [15]. There are also a few helpful rules of thumb that can also be useful in designing the inductors found in [16]. Since the side of the inductor that contains the underpass has a slightly lower Q, it was connected to ac ground in the oscillator [15]. It should be noted as well that when inductors are used differentially, they can have much higher Q's [17] and future work will use these more optimal structures.

IV. Experimental Results

The complete receiver front-end chip using ground-shielded inductors is shown in Fig. 4. The chip was fabricated in Nortel Networks' 0.5-μm bipolar process with 25-GHz f_T. The VCO is shown in the bottom right-hand-side corner. A second version of the receiver was also fabricated for comparison that used only standard inductors.

Care was taken to ground the substrate around the VCO in order to minimize the coupling of the VCO signal to other parts of the receiver. As well, all differential signals in the circuits were kept as symmetric as possible to avoid unwanted phase shifts. On the right-hand side of the chip, the pads labeled $\mathrm{LO}+$ and $\mathrm{LO}-$ are included for testing purposes only. This allows for the direct observation of the VCO output and provides the ability to measure the output power and phase noise. The RF input is shown to the left-hand side and the differential IF output pads are indicated on the top. Numerous ground pads are distributed all around the periphery to ensure minimum inductance to ground. The entire receiver occupies a die area of 2.13 mm $\times$ 1.75 mm, which made it possible to use a 20TQFP package for this design.

There were many on-chip inductors designed for use in the receiver. The inductors used in the design of the VCO are of particular interest due to their impact on the VCO performance. Test structures used to compare the relative performance of the ground-shielded to regular inductors were built. Measurements for the inductor used in the VCO with and without a ground shield are shown in Fig. 5. Note that the ground shield gives an improvement in Q of about 30% over the standard structure; however, the self-resonance of this structure is also lower. This is due to the increased capacitance because of the presence of the shield.

TABLE I
Comparison of Receiver Front-End Performance

	Receiver with Off-Chip VCO	Receiver with VCO	Receiver with shielded VCO
IF Frequency	300MHz	300MHz	300MHz
RF Frequency	1.9GHz	1.9GHz	1.9GHz
VCO Tuning Range	N/a (off chip)	2.09-2.30GHz	2.04-2.24GHz
Notch Tuning	2.34-2.55GHz	2.34-2.55GHz	2.34-2.55GHz
NF @ 1.9GHz	4.5dB	4.8dB	4.5dB
Conversion Gain	28.8dB	24.9dB	25.6dB
VCO Phase Noise @100kHz offset	N/a (off chip)	-100dBc/Hz	-103dBc/Hz
S_{11}	-19dB	-10.8dB	-12.5dB
Image Rejection	>65dB	>65dB	>65dB
RF-IF Isolation	32.9dB	28dB	31dB
LO-RF Isolation	61dB	55.7dB	52.7dB
LO-IF Isolation	37.5dB	46.7dB	44.7dB
Input IP3	-19dBm	-19dBm	-19dBm
Power Supply	3.0V	3.0V	3.0V
DC Current	16.1mA	32.5mA	32.5mA
Package	20TQFP	20TQFP	20TQFP

Care had to be taken when integrating the VCO with the rest of the circuits. Since the mixer LO input and the VCO output had different dc-bias requirements, a coupling capacitor C_C had to be added in series with the VCO output. Ideally, this capacitor should be large to minimize the signal loss. However, in practice, making this device large increases the coupling of the VCO signal into the substrate. As a compromise, C_C was made 3 pF. Signal loss was also minimized by adjusting the mixer bias network (R_{22} and R_{23}) so as to provide a high input impedance (350 Ω), giving the VCO the luxury of driving an impedance higher than 50 Ω.

The two versions of the 2.2-GHz VCO were biased identically. The core and buffer of each VCO drew 7 mA of current. The measured differential output power of the VCO with standard inductors was -5.3 dBm and the VCO that used ground-shielded inductors produced -4.3 dBm of output power, measured while driving 50 Ω. However, when driving the much higher input impedance of the mixer quad (see Fig. 2), simulations showed that the signal swing was higher and with sufficient amplitude to drive the quad. The VCOs had a tuning range of 220 MHz (10%) for 2.3 V of tuning voltage variation.

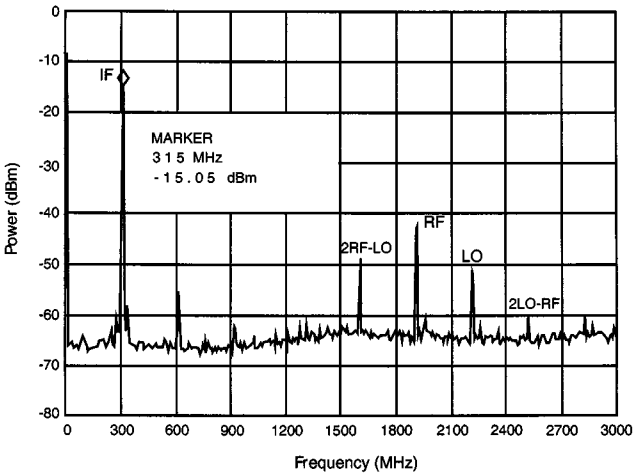

Fig. 7. Differential IF output spectrum for the receiver front-end using standard inductors in the VCO with a −40-dBm RF input at 1.9 GHz.

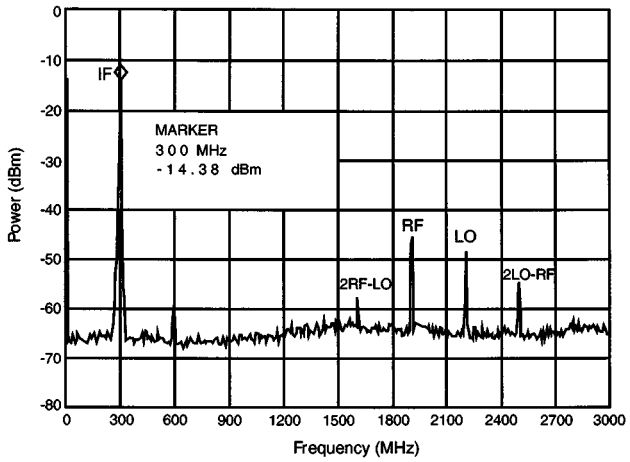

Fig. 8. Differential IF output spectrum for the receiver front-end using ground-shielded inductors in the VCO with a −40-dBm RF input at 1.9 GHz.

The improved inductors also had a positive impact on the phase noise of the VCOs. A plot of the relative phase noise of the two designs is shown in Fig. 6. The ground shield improved the phase noise by about 3 dB from −100 dBc/Hz at 100-kHz offset for the VCO using standard inductors to −103 dBc/Hz at 100-kHz offset for the VCO using the ground-shielded inductors. This phase noise of −103 dBc/Hz is equivalent to −118 dBc/Hz at 600-kHz offset. Simple hand calculations using (5)–(7) predict almost the same phase-noise variations. They predicted −5.41- and −4.25-dBm output power and a phase noise of −95.3 and −98.0 dBc/Hz at 100-kHz offset for the nonground-shielded and ground-shielded versions of the VCO, respectively.

Numerous measurements were also performed on the receivers themselves. The LNA was input matched using a 3.9-nH off-chip series inductor. S_{11} was better than −10 dB for both versions of the receiver. Table I summarizes the figures-of-merit for the system and compares them against a previous version of the receiver front-end with the off-chip VCO producing 0-dBm output power. The IF output spectrum for both versions of the receiver are shown in Figs. 7 and 8 for a 1.9-GHz RF input power of −40 dBm.

From Table I, it is easy to see that it is advantageous to use ground-shielded inductors for the VCO. The ground-shielded VCO had better phase noise, and higher output power, which led to a better NF and higher gain for the receiver. The only minor penalty (when compared with the unshielded version) is an increased LO coupling to the other ports. This is, in part, due to increased LO power and, in part, due to some leakage from the ground shield through the ground metal that runs all over the chip. It is important to note here that this LO leakage represents a worst case, as the entire chip shared common ground metal. Future experiments should insure that the VCO has separate ground pins, further isolating it from the rest of the circuit and further improving the LO isolation. As well, the coupling capacitors between the VCO and mixer may have caused some LO signal to leak into the substrate. However, the isolations are still very good. For example, the LO–IF isolation is better than the receiver with an off-chip VCO. This is most likely because off-chip VCOs experience coupling through the bond wires and packaging. Note that no bond wires were connected to the LO pins in Fig. 4. These pins were used for preliminary wafer probing measurements on the VCOs only.

The NF was measured for both versions of the receiver front-end, and found to be better for the receiver with the ground-shielded VCO. The NF of the receiver using ground-shielded inductors is identical to the receiver with an off-chip VCO. The conversion gain of the receiver with a ground-shielded VCO is lower than for the receiver with an off-chip VCO due to the lower power generated by the monolithic VCO. However, it is sufficient for a typical application.

The bias current reported in Table I does not include the current drawn by the IF output buffers. The buffer in an actual application would require lower current because the receiver would most likely drive a high impedance.

V. Conclusion

A completely monolithic receiver front-end has been presented in this paper. The receiver has an on-chip tunable image-reject filter and VCO. The image filter is guaranteed to be stable under normal operation. Two versions of the VCO were integrated with the receiver front-end. One VCO used standard square on-chip inductors, while the other used inductors with ground shields. The use of ground shields reduced the phase noise of the VCO by 3 dB. This version of the receiver has 25.6 dB of conversion gain and a NF of 4.5 dB. Moving the VCO on-chip also showed that LO–IF isolation was improved by almost 10 dB in both versions. As well, since this design requires no off-chip components and it occupies a die area of only 2.1 mm × 1.75 mm, it would be ideal for dual- or triple-band applications where several receiver front-ends would be integrated on one chip.

Acknowledgment

The authors would like to thank Dr. J. Ojha, Nortel Networks, Ottawa, ON, Canada, for providing technology access.

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The Summation-by-Parts Algorithm—A New Efficient Technique for the Rapid Calculation of Certain Series Arising in Shielded Planar Structures

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***Abstract*—This paper presents a new technique for the convergence acceleration of a large class of series often arising in electromagnetic problems. The technique is based on the recursive application of the integration-by-parts technique to discrete sequences, thus the given name of the "summation-by-parts" technique. It is shown that the new technique greatly enhances the convergence rate of the series treated, and very small relative errors are obtained by performing a few simple operations. The new technique is applied to the efficient numerical calculation of the Green's functions in a parallel-plate waveguide.**

***Index Terms*—Convergence acceleration, modal expansions, shielded Green's functions.**

I. Introduction

In many electromagnetic problems, the relevant physical quantities (electric and magnetic fields) and associated quantities (potentials) are expressed in terms of infinite series that are usually very slow convergent. This is the case, for instance, when analyzing shielded circuits [1], cavity-backed antennas [2], or microwave devices inside photonic crystals [3]. In these problems, the need of numerically evaluating infinite sums, usually very time-consuming, prevents, in general, the development of efficient software codes.

To try to overcome this difficulty, several convergence series acceleration techniques have been developed in the past. Detailed and complete survey on series acceleration is available in any modern textbook (see, e.g., [4]).

As for the application of these general methods to the acceleration of series arising in electromagnetic problems, a very interesting work can be found in [5]. In that paper, some results on series acceleration are given when these techniques are applied to the numerical evaluation of the free-space periodic Green's functions, and to the evaluation of the quasi-static Green's function term developed within the complex images representation derived in [6].

Other acceleration techniques employed in the past include the use of the Poisson's summation formula together with the Kummer's transformation for the evaluation of the shielded Green's functions [7], [8] and the Ewald transformation, which was used in [9] for the same purpose.

In spite of all these efforts, the use of these techniques in a reliable systematic fashion is not straightforward, and some situations and geometries can be found where the efficiency of the algorithms breaks down. In this context, this paper describes an alternative algorithm to accelerate the convergence behavior of certain series often arising in electromagnetic problems. It is shown in this paper that the new technique can be applied in a reliable fashion, and greatly accelerates the convergence rate of the series treated.

II. Theory

In many microwave circuits involving multilayered planar shielded configurations, the relevant Green's functions of the problem can be formulated in terms of very slow convergent modal series of the form

$$S_\infty = \sum_{n=0}^{\infty} \tilde{G}_n f_n \tag{1}$$

where $\tilde{G}_n$ represents the spectral-domain Green's function of the problem, which it is a slow varying function, and f_n, which is a highly oscillatory (typically sinusoidal) function. In this section, we will present the mathematical transformations leading to the new formulation for the convergence acceleration of the series whose general form is shown in (1).

To start, we first define partial sums and reminders of the original series as follows:

$$\begin{aligned} S_{N-1} &= \sum_{n=0}^{N-1} \tilde{G}_n\, f_n \\ R_N &= \sum_{n=N}^{\infty} \tilde{G}_n\, f_n \\ S_\infty &= S_{N-1} + R_N \end{aligned} \tag{2}$$

and since the partial sums S_{N-1} are bounded, the attention must be focused in the efficient evaluation of the infinite remainder R_N. To do so, we apply simple algebraic manipulations to the remainder R_N in (2), allowing us to rewrite it as

$$R_N = \sum_{n=N}^{\infty} \tilde{G}_n\, f_n = \tilde{G}_N \sum_{n=N}^{\infty} f_n + \sum_{n=N}^{\infty} \left[\left(\tilde{G}_{n+1} - \tilde{G}_n \right) \left(\sum_{k=n+1}^{\infty} f_k \right) \right]. \tag{3}$$

Manuscript received April 5, 2000.

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Publisher Item Identifier S 0018-9480(02)00735-4.